CLAIMS

What is claimed is:

1. A processor subsystem for transacting data, the processor subsystem comprising:

a memory for storing data, the memory mapped to a first address space associated with data values with a first length and a second address space associated with data values with a second length; and

a bridge for performing one transaction after receiving a transaction with an address corresponding to the first address space and for performing two or more transactions after receiving a transaction with the address corresponding to the second address space.

2. The processor subsystem of claim 1, wherein the bridge further comprises:

address control logic for causing the bridge to perform one transaction after receiving a transaction with an address corresponding to the first address space and perform two or more transactions after receiving a transaction with the address corresponding to the second address space.

3. The processor subsystem of claim 2, wherein the address decode logic comprises:

a first logic circuit for decoding the address; and

a second logic circuit for determining if address corresponds to the first address space or the second address space.

4. The processor subsystem of claim 3, wherein the second logic circuit determines whether the address corresponds to the first address space or the second address space by examining a particular bit in the address.

5. Processor subsystem of claim 1, wherein the first length is 16 bits and the second length is 32 bits.

6. A method for transacting data, said method comprising:

receiving a transaction for a target address;

performing one transaction if the target address corresponds to a first address space; and

performing two transactions if the target address corresponds to a second address space.

7. The method of claim 5, further comprising:

decoding the target address.

8. The method of claim 5, further comprising:

determining whether the address corresponds to the first address space or the second address space by examining a particular bit in the address.

9. A circuit for transaction data, said circuit comprising:

a processor subsystem comprising:

memory for storing data, the memory mapped to a first address space associated with data values of a first length and a second address space associated with words of a second length; and

a bridge for performing one transaction after receiving a transaction with an address corresponding to the first address space and for performing two or more transactions after receiving a transaction with the address corresponding to the second address space; and

a processor for requesting transactions from the processor subsystem.

10. The circuit of claim 9, wherein the bridge further comprises:

address control logic for causing the bridge to perform one transaction after receiving a transaction with an address corresponding to the first address space and perform two or more transactions after receiving a transaction with the address corresponding to the second address space.

11. The circuit of claim 10, wherein the address decode logic comprises:

a first logic circuit for decoding the address; and

a second logic circuit for determining if address corresponds to the first address space or the second address space.

12. The circuit of claim 11 wherein the second logic circuit determines whether the address corresponds to the first address space or the second address space by examining a particular bit in the address.

13. The circuit of claim 9, wherein the first length is 16 bits and the second length is 32 bits.

14. The circuit of claim 9, further comprising:

a bus for transmitting the transaction from the processor to the processor subsystem.